

**REMARKS**

The Abstract has been amended to address objections raised by the examiner.

Claim 1 has been replaced, thereby overcoming the double patenting rejections. Further, a terminal disclaimer with respect to all patents to which this application claims priority is attached.

During recent license discussions, a potential licensee has referred to figure 40 of previously cited patent 5,602,771 with reference to the cross coupled NOR gates. The circuit of a typical NOR gate can be seen in the attached reference, Weste, Neil H. E., *et al.*, "Principles of CMOS VLSI Design," *Addison-Wesley Publishing Company*, page 13 (1998). The pending claim distinguishes the NOR gate implementation at least in that claim 2 recites cross coupled transistors connected drain-to-gate.

**Information Disclosure Statement**

A Supplemental Information Disclosure Statement (SIDS) is being filed concurrently herewith. Entry of the IDS is respectfully requested.

It is believed that the claim is in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,  
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By 

James M. Smith

Registration No. 28,043

Telephone: (978) 341-0036

Facsimile: (978) 341-0136

Concord, MA 01742-9133

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